

## **TS-EPON-OLT**

OLT for IEEE 802.3ah-2004 PX-20+
1.25Gbps Downstream and 1.25Gbps Upstream

#### **Features**

- · SFP Package with SC connector
- 1.25Gbps, 1310nm BM APD Receiver
- 1.25Gbps, 1490nm Transmitter
- Compliant With IEEE 802.3ah-2004
- Up to 20km distance at 9/125µm G.652 SMF
- Complies with RoHS directive (2002/95/EC)
- Operating case temperature: Standard: 0 to +70°C



### **Applications**

- EPON 20km OLT Side
- Access Networks
- Fiber to the Home, Curb, Office(FTTx)

#### Description

TONGSION's high performance EPON OLT transceiver module is designed for Passive Optical Network application, 1.25Gbps downstream and 1.25Gbps upstream. It is fully compliant with IEEE 802.3ah-2004.

The EPON OLT transceiver is packaged of small form factor pluggable with SC connector. The digital diagnostic monitoring function is fully compliant with SFP MSA.

The module consists of 1490nm DFB Laser, APD detector and WDM filter in a high-integrated optical sub-assembly. It transmits 1.25Gbps at 1490nm, and receives 1.25Gbps at 1310nm in burst mode.





# **Absolute Maximum Ratings**

Parameter	Symbol	Min.	Max.	Units	Notes
Storage Temperature	Tst	-40	+85	°C	-
Operating Humidity	RH	5	90	%	Non-condensing
Supply Voltage	Vcc	0	4.0	V	

## **Recommended Operating Conditions**

Parameter	Symbol	Min	Typical	Max	Unit
Operating Case Temperature	Tc	0	-	+70	°C
Power Supply Voltage	Vcc	3.13	3.3	3.47	V
Power Supply Current	lcc	-	-	300	mA
Date Rate	Upstream/Downstream		1.25/1.25		Gbps

## **Electrical Characteristics**

Parai	neter	Symbol	Min	Typical	Max	Unit	Notes
			Transmitte	er			
LVPECL C Inputs(Di		Vin	200		1600	mVpp	AC coupled internally
Power Sup	ply Current	lcc_Tx			200	mA	
· ·	pedance ential)	Zin	90	100	110	ohms	Rin > 100 kohms @ DC
Tx Disable			2		Vcc	V	
Tx Enable			0		0.8	V	
Tx Fault_High			2.4		Vcc	V	
Tx Fault_Normal			0		0.4	V	
	Receiver						
	Outputs ential)	Vout	400		1600	mVpp	DC coupled outputs
Power Supply Current		lcc_Rx			150	mA	
Dv 100	High		2		Vcc	V	
Rx_LOS	Low		0		0.8	V	





**Optical Characteristics** 

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Date Rate (Upstream/Downstream)			1.25/1.25		Gbps	
9µm Core Diameter SMF			20		km	
		Transmitte	er			
Centre Wavelength	λс	1480	1490	1500	nm	
Spectral Width (-20dB)	Δλ			1	nm	
Side Mode Suppression Ratio	SMSRR	30			dB	
Average Output Power	P out	2		7	dBm	1
Downstream optical penalty				1	dB	
Extinction Ratio	ER	9			dB	2
Tolerance to Tx back reflection		-15			dB	
Rise/Fall Time(20%~80%)	tr/tf			160	ps	2,3
Output Optical Eye		IEEE 802.3ah Compliant				
Optical Output Power with TX OFF	P_off			-40	dBm	
		Receive	r			
Centre Wavelength	λс	1260	1310	1360	nm	
Receiver Sensitivity	Pmin			-30	dBm	4
Receiver Overload	Pmax	-6			dBm	4
Receiver Burst-Mode Dynamic Range		15	20		dB	5
Receiver Reflectance	CR			-20	dB	
LOSS Assert Level	LOSA	-44			dBm	
LOSS De-Assert Level	LOSD			-32	dBm	
Signal Detect Hysteresis		0.5		6	dB	
Receiver Settling Time	Ts			400	ns	
Damage Threshold for Receiver	Pin, damage	3			dBm	
Maximum Receiver Reflectance	Rx_r			-20	dB	

#### Notes:

- 1: Measured with 9/125um G.652 SMF.
- 2: Filtered, Measured with PRBS2<sup>7</sup>-1 test pattern @1.25Gbps.
- 3: Measured with the Bessel-Thompson filter OFF.
- 4: Measured with a PRBS 2<sup>7</sup> -1 test pattern @1.25Gbps, BER 1X10<sup>-12</sup>.
- $5: The \ input power \ difference \ between \ two \ subsequent \ high \ and \ low \ burst \ data.$

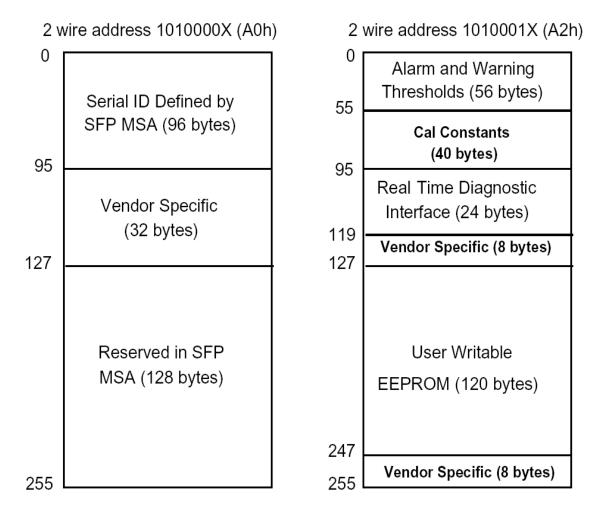


## Digital Diagnostic Memory Map

The transceivers provide serial ID memory contents and diagnostic information about the present operating conditions by the 2-wire serial interface (SCL, SDA).

The diagnostic information with internal calibration or external calibration all are implemented, including received power monitoring, transmitted power monitoring, bias current monitoring, supply voltage monitoring and temperature monitoring.

The digital diagnostic memory map specific data field defines as following.





## Pin Diagram

20	VEET
19	TD-
18	TD+
17	VEET
16	VCCT
15	VCCR
14	VEER
13	RD+
12	RD-
11	VEER

VEET
TX FAULT
TX DISABLE
MOD -DEF(2)
MOD -DEF(1)
MOD -DEF(0)
RESET
BSD
RSSI TRIG.
VEER

Top of Board Bottom of Board

## **Pin Descriptions**

Pin	Signal Name	Description	Plug Seq.	Notes
1	$V_{EET}$	Transmitter Ground	1	
2	TX FAULT	Transmitter Fault Indication	3	Note 1
3	TX DISABLE	Transmitter Disable	3	Note 2
4	MOD_DEF(2)	SDA Serial Data Signal	3	Note 3



#### **SFP Series**

5	MOD_DEF(1)	SCL Serial Clock Signal	3	Note 3
6	MOD_DEF(0)	TTL Low	3	Note 3
7	RESET	LVTTL input. Assert "Reset" high at the end of previous burst,16 bits in	3	Note 4
8	BSD	Burst signal detect	3	Note 5
9	RSSI TRIG.	CMOS input. Assert high at the beginning of the monitored burst	3	Note 6
10	$V_{EER}$	Receiver ground	1	
11	$V_{EER}$	Receiver ground	1	
12	RD-	Inv. Received Data Out	3	Note 7
13	RD+	Received Data Out	3	Note 7
14	$V_{EER}$	Receiver ground	1	
15	$V_{CCR}$	Receiver Power Supply	2	
16	V <sub>CCT</sub>	Transmitter Power Supply	2	
17	V <sub>EET</sub>	Transmitter Ground	1	
18	TD+	Transmit Data In	3	Note 8
19	TD-	Inv. Transmit Data In	3	Note 8
20	V <sub>EET</sub>	Transmitter Ground	1	

#### Notes:

Plug Seq.: Pin engagement sequence during hot plugging.

- 1) TX Fault is an open collector output, which should be pulled up with a 4.7k~10kΩ resistor on the host board to a voltage between 2.0V and Vcc+0.3V. Logic 0 indicates normal operation; Logic 1 indicates a laser fault of some kind. In the low state, the output will be pulled to less than 0.8V.
- 2) TX Disable is an input that is used to shut down the transmitter optical output. It is pulled up within the module with a  $4.7k\sim10k\Omega$  resistor. Its states are:

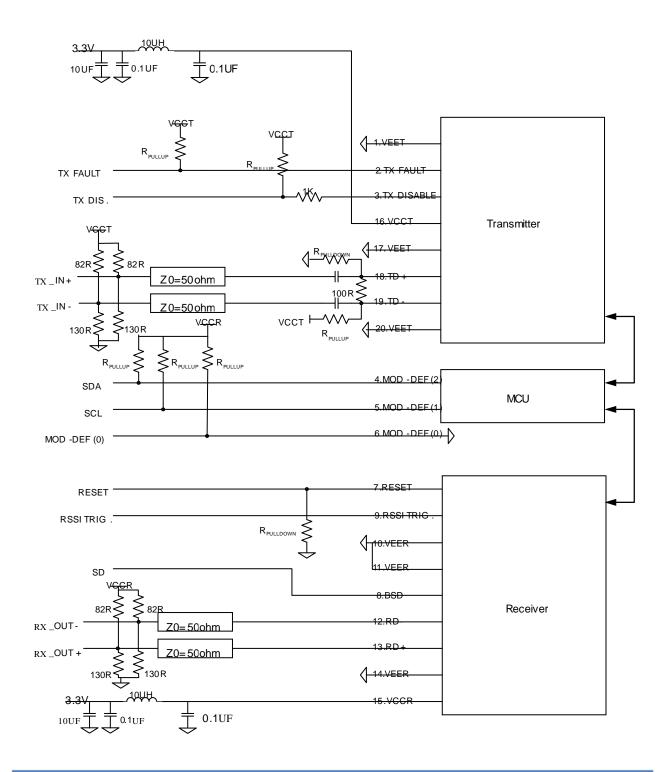
 $\begin{array}{lll} \mbox{Low (0 to 0.8V):} & \mbox{Transmitter on} \\ \mbox{(>0.8V, < 2.0V):} & \mbox{Undefined} \end{array}$ 

High (2.0 to 3.465V): Transmitter Disabled Open: Transmitter Disabled

- 3) Mod-Def 0,1,2. These are the module definition pins. They should be pulled up with a 4.7k~10kΩ resistor on the host board. The pull-up voltage shall be VccTor VccR.
  - Mod-Def 0 is grounded by the module to indicate that the module is present
  - Mod-Def 1 is the clock line of two wire serial interface for serial ID
  - Mod-Def 2 is the data line of two wire serial interface for serial ID
- 4) RESET is a LVTTL input. When the previous burst signal package is end, the host will give a "high" RESET to restore the state of LA. Internal pull-down 10K resistor to GND.
- 5) BSD can track the state of receiving burst signal. Logic 0 indicates loss of signal; Logic 1 indicates receiving signal packages.
- 6) RSSI TRIG is a CMOS input. Assert high after 30ns delay time of the beginning of the monitored burst package, at least 300ns in duration.
- 7) RD-/+: These are the differential receiver outputs. They are internally DC-coupled 100 differential lines which should be terminated with 100Ω (differential) at the user SERDES.
- 8) TD-/+: These are the differential transmitter inputs. They are internally AC-coupled, differential lines with 100Ω differential termination inside the module.



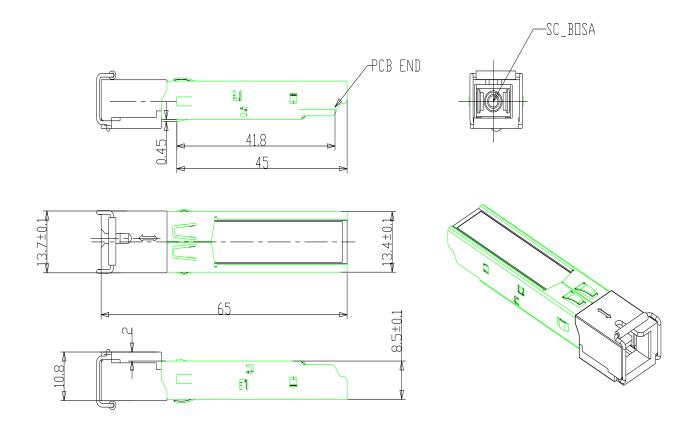
#### **Recommended Interface Circuit**







#### **Mechanical Dimensions**





### Ordering information

Part Number	Product Description		
TS-EPON-OLT	Tx1490nm/Tx1310nm, 1.25Gbps/1.25Gbps, SC, 20km, 0°C~+70°C, With DDM		

#### **Important Notice**

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